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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/501,977	02/11/2000	Yoshitaka Takahashi	500.38174X00	4612

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EXAMINER
WHITMORE, STACY

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 09/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/501,977	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Stacy A Whitmore	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Barrientos (5,910,899).

3. As for claim 18-19, Barrientos disclosed the invention as claimed, including an information processing system used for designing a semiconductor integrated circuit [abstract, lines 1-2], comprising:

a storing unit for storing circuit information of a module constituting the semiconductor integrated circuit, a floorplan which is allocation information of blocks constituting the module, and evaluation indices, generated based on said circuit information of the module, for evaluating modifications of the floorplan [abstract, fig. 5; col. 3, lines 51-53; and col. 4, lines 54-65; col. 5; Barrientos evaluation indices are generated based on said circuit information of the module, see col. 2, lines 41-43, col. 9, lines 28-34];

wherein the circuit information, floorplan and evaluation indices are associated with each other [cols. 5 and 8]; and

an input/output unit for transmitting the associated circuit information, floorplan and evaluation indices from the storing unit [the input output unit is inherently included in Barrientos system because Barrientos system utilizes a computer program product that is interactive with a user, and further displays information relating to the interaction, which would require the use of an input output unit in order to perform those functions, see cols. 3, 5, and 8].

[claim 19] Barrientos further taught wherein the evaluation indices includes know-how of a designer who designs a semiconductor integrated circuit [col. 22, lines 33-41].

4. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barrientos (5,910,899) in view of Ramachandran (6,002,857).

5. As for claim 16, Barrientos disclosed the invention as substantially claimed, including an information processing system, comprising:

an input unit for receiving, from external of said information processing system, circuit information of a module constituting a semiconductor integrated circuit, a floorplan which is allocation information of blocks constituting the module, and evaluation indices, generated based on said circuit information of the module, for evaluating modifications of the floorplan [abstract, fig. 5; col. 3, lines 51-53; and col. 4, lines 54-65; col. 5: the input output unit is inherently included in Barrientos system because Barrientos system utilizes a computer program product that is interactive with a user, and further displays information relating to the interaction, which would require the use of an input output unit in order to perform those functions, see cols. 3, 5, and 8: see col. 8, lines 36-38, col. 22, lines 53-61 for the external input of circuit information, floorplan, and evaluation indices; Barrientos evaluation indices are generated based on said circuit information of the module, see col. 2, lines 41-43, col. 9, lines 28-34];

wherein the circuit information, floorplan and evaluation indices are associated with each other [abstract, fig. 5; col. 3, lines 51-53; and col. 4, lines 54-65; col. 5];

a storing unit for storing the associated circuit information, floorplan, and evaluation indices [abstract, fig. 5; col. 3, lines 51-53; and col. 4, lines 54-65; col. 5]; and

a processing unit for reading the floorplan stored in the storing unit according to the specification information for modifying the floorplan when the specification information for modifying the floorplan is input, generating a floorplan candidate being modified based on the read floorplan and the specification information, evaluating the generated floorplan candidate based on the evaluation indices stored in the storing unit, and selecting one floorplan based on an evaluation result [abstract, fig. 5; col. 3, lines 51-53; and col. 4, lines 54-65; col. 5; see also col. 2, lines 41-43, col. 9, lines 28-34].

Barrientos did not specifically teach generating a plurality of floorplans, and selecting one of the floorplans based on the evaluation result.

Ramachandran dislcosed the generation of a plurality of floorplans and user selection selection of one of the plurality of candidate floorplans based on evaluation result [abstract].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Barrientos and Ramachandran because adding the generation of a plurality of floorplans and user selection selection of one of the plurality of candidate floorplans based on evaluation result would improve Barrientos' system by allowing user choice of a floorplan which best suites design criteria of evaluated indices[see Ramachandran, abstract] which would improve the overall design integrity of Barrientos' floorplan circuit design.

6. Applicant's arguments filed June 10, 2003 have been fully considered but they are not persuasive.

Applicant argues in substance on pages 4-8 of the remarks:

A: Barrientos does not disclose the limitation "a module designer creates the evaluation indices and a system LSI designer creates the floorplan".

B: Barrientos nor Ramachandran do not disclose a system for receiving input externally, circuit information of a module...,a floorplan..., and evaluation indices, generated based on the circuit information of the module, for evaluating modifications of the floorplan.

C: The combination of Barrientos in view of Ramachandran did not disclose generating a plurality of floorplans and selecting one of the floorplans based on the evaluation result.

Examiner disagrees for the following reasons:

As to point A: The argument that Barrientos does not disclose the limitation "a module designer creates the evaluation indices and a system LSI designer creates the floorplan" is moot because the limitation is not claimed.

As to point B: Barrientos disclosed a system for receiving input externally, circuit information of a module...,a floorplan..., and evaluation indices, generated based on the circuit information of the module, for evaluating modifications of the floorplan [see as cited in the rejection of claims 16 and 18, especially newly emphasized columns 2 and 9, where the examiner points the evaluation indices that are generated based on said circuit information of the module, see col. 2, lines 41-43, col. 9, lines 28-34.

As to point C: The combination of Barrientos in view of Ramachandran did disclose generating a plurality of floorplans and selecting one of the floorplans based on the evaluation result. Examiner relies on Barrientos for the claimed limitations except for generating a plurality of floorplans and selecting one of the floorplans. Ramachandran disclosed selecting one of a plurality of candidate floorplans based on an evaluation result [abstract].

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy A Whitmore
Patent Examiner

Art Unit 2812

SAW